REMARKS

Claims 1-9, 21-24, 35-38, and 49-52 are pending in the present application. In the Office Action, claims 1, 3, 6, 21-24, 35-38, and 49-52 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Hotley (U.S. Patent No. 5,442,704) in view of Gephardt, et al (U.S. Patent No. 5,623,673. Claims 4, 7-8, and 26-27 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Hotley and Gephardt in view of Gafken (U.S. Patent No. 6,026,016). Claims 2, 5, and 28 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Hotley and Gephardt in view of Watts (U.S. Patent No. 6,816,925). The Examiner's rejections are respectfully traversed.

To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. That is, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01.

Hotley describes a secure memory card that includes a security access control unit and a chip memory. The chip memory is organized into a number blocks having a number of rows, and each row includes a single lock bit location that may provide storage for lock bits within each block. The security access control unit may perform a predetermined key validation

operation for a protected block by serially comparing bits of the key value against the bit contents of the lock bit positions of the memory block. See Hotley, col. 3, ll. 4-27. However, as admitted by the Examiner, Hotley is completely silent with regard to a system management mode (SMM). As stated in the specification of the present application, System Management Mode (SMM) is a mode of operation in the computer system that was implemented to conserve power. The SMM was created for the fourth generation x86 processors. See Patent Application, page 15, ll. 13-17.

The Examiner relies upon Gephardt to describe a system management mode for use in a computing system 200. Gephardt describes a lock-out register 216 that may be used for locking a system management space 410 used to store system management routines. After the system management routines are loaded into the system management space 410, the lock-out register 216 is set such that the system management routines cannot be overwritten during a normal mode of operation. Once the lock-out register 216 is set by system software it cannot be subsequently reset while the system is in the normal mode. The system management space 410 can be accessed while operating in the system management mode or the debug system management mode regardless of the state of the lock-out register. See Gephardt, col. 9, ll. 1-27.

The Examiner then alleges that a person of ordinary skill in the art would be motivated to implement the lock-out registers 216 described by Gephardt in the smart card described by Hotley to restrict access to system management routines. Applicants respectfully disagree for at least the following reasons. First, Applicants respectfully submit that the cited references provide no suggestion or motivation for implementing a system management mode on a smart card. In particular, the cited references provide no indication that smart cards require any of the power management functions that may be provided in the system management mode. Second,

Applicants respectfully submit that a person of ordinary skill in the art would not use the memory rows described by Hotley to store system management routines or any other routine. In particular, routines are not generally stored in a row-by-row structure and therefore protecting individual rows using a lock bit (as described by Hotley) would inhibit operation of these routines. Third, Applicants respectfully submit that a person of ordinary skill in the art would not implement the lock-out registers 216 described by Gephardt on the smart card described by Hotley at least in part because the lock-out registers 216 *completely* block access to the protected memory during a normal mode of operation, whereas the smart card described by Hotley is designed to allow access to protected registers following an authentication procedure.

The Examiner relies on Gafken to describe a read lock bit, a write lock bit, and a lockdown bit. The Examiner also relies upon Watts to describe a low pin count (LPC) bus protocol. However, both Gafken and Watts are completely silent with regard to a system management mode. Consequently, neither Gafken nor Watts remedies the fundamental deficiencies of Hotley and Gephardt.

For at least the aforementioned reasons, Applicants respectfully submit that the prior art of record fails to provide any suggestion or motivation to combine the cited references in the manner suggested by the Examiner to arrive at the claimed invention. Applicants therefore respectfully submit that the Examiner has failed to make a *prima facie* case that the present invention is obvious over the prior art of record. Applicants request that the Examiner's rejections of claims 1-9, 21-24, 35-38, and 49-52 under 35 U.S.C. 103(a) be withdrawn.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the

undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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